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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,192	01/28/2004	Chun Ho Fan	50626.67	9840

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EXAMINER	
LEE, CALVIN	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/765,192	FAN et al.	
	Examiner	Art Unit	
	Lee, Calvin	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

OFFICE ACTION

General Information

1. The drawings and the IDS dated 01/28/04 have been approved.

Claim Rejections - 35 U.S.C. § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having skills in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 7-9, and 12-13 are rejected under 35 U.S.C. 103(**a**) as being unpatentable over *Islam et al* (US 6,812,552) in view of *Wang et al* (US 6,872,591).

The Examiner notes that since *Islam et al* discloses, "the bottom surface is etched entirely through the film to isolate the lead contacts from the chip-pad and each other" [col. 7, ln.38], *Islam et al* inherently teaches or suggests a leadless chip carrier, comprising the steps of:

-selectively/partially etching at least a first/top surface of a leadframe strip **100** to define at least a plurality of contact pads **113** and a die attach pad **115** [Fig. 6 and col. 8, ln.35];

-selectively plating at least one layer of metal on a second/bottom surface (i.e., the undersurface of the contact pads and die attach pad) of the leadframe strip [col. 8, ln.28];

-mounting a semiconductor die **140** on the partially defined die attach pad [Fig. 7 and col. 9, ln.18]

-wire bonding the semiconductor die to ones of the contact pads [Fig. 8 and col. 9, ln.22];

-encapsulating the wire bonds and the semiconductor die in a molding material **170**, which covers a top portion of the die attach pad and of said contact pads [Fig. 9 and col. 9, ln.33];

-selectively etching a second surface of the leadframe strip, to define a bottom portion of the contact pads and of the die attach pad, by etching the second surface with at least one layer of metal resisting etching [see "back etching the metal" in Fig. 10 and col. 9, ln.49];

-and singulating the leadless chip carrier from the leadframe strip **100** [Fig. 11 and col. 9, ln.60]

a) In re claim 1, *Islam et al* discloses, "a chip microcarrier that is later joined to the plastic substrate," but not explicitly teach or suggest the chip carrier being a plastic chip carrier. *Wang et al* discloses, "the conductive terminals can be configured so that the assembly is a surface mount technology package such as a plastic leadless chip carrier" [col. 58, ln.50].

It would have been obvious to one having skills in the art to have modified the chip carrier of *Islam et al* by utilizing a plastic chip carrier for the purpose of being no more metal to cut through and no other problems associated with cutting plastic and metal in combination.

b) In re claim 2, since *Islam et al* suggests "metal strip **100** is pre-plated on both the front side and the back side prior to the photolithographic patterning" [col. 8, ln.21], *Islam et al* inherently teaches plating at least one layer of metal on the strip's first surface prior to (subsequent process steps including the step of) mounting the semiconductor die.

c) In re claim 3, since *Islam et al* suggests preplating the whole leadframe strip ... that enables bonding as well as solderability [col. 8, ln.21], *Islam et al* inherently teaches selectively plating at least one layer of metal on a peripheral portion of the top surface of the die attach pad and of the contact pads for facilitating ground wire bonding to the die pad and the contact pads.

d) In re claim 4, *Islam et al* is silent about a single plating step. Nevertheless, such single plating step is known in the semiconductor plating as evidenced by *Wang et al* disclosing "the connection joint ... can be simultaneously formed during a single plating operation" [col. 8, ln.41]

It would have been obvious to one having skills in the art to have modified the plating process by utilizing a single plating step for the purpose of ensuring stable and reliable mechanical interconnection of pad on pad and reducing manufacturing time and cost.

e) In re claims 7 and 12, *Islam et al* suggests plating the layer of metal selected from the group consisting of a layer of Ag, Ni/Au, and Ni/Pd [col. 8, ln.27].

f) In re claims 8 and 13, since *Islam et al* suggests preplating the whole leadframe strip [col. 8, ln.21], *Islam et al* inherently teaches plating a perimeter portion of the leadframe strip, wherein the perimeter portion will be removed by the subsequent step of singulating the structure.

4. Claims 5-6 and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Islam et al* in view of *Wang et al*, and further in view of *Stork* (US 3,622,385).

Islam et al discloses that coating the bottom portion of the die attach pad and contact pads comprises dipping at least a portion of the leadless chip carrier in an "immersion-tin electroless-nickel" [col. 8, ln.30]. However, *Islam et al* does not teach or suggest such coating for oxidation protection. *Stork* suggests providing connection pads **8** with a layer of silver to protect the copper pads against oxidation [Fig. 2 and col. 4, ln.15].

It would have been obvious to one having skills in the art to have modified the plating process by utilizing a single plating step for the purpose of protecting the underlying plated pad from oxidation.

Contact Information

5. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896 on Mondays thru Thursdays 6:30-4:30 (EST). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2818's Supervisory Patent Examiner *David Nelms* can be reached at (571) 272-1787. The central fax number for the organization (where this application is assigned to) is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system at http:/pair-direct.uspto.gov. Should you have questions on access to the PAIR system, contact the Electronic Business Center at (866) 217-9197.

Calvin Lee

Date: July 25, 2005